UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,921	07/09/2003	Takahisa Hatakeyama	826.1880	7868

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EXAMINER
SHERR, CRISTINA O

ART UNIT	PAPER NUMBER
3685	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/614,921	HATAKEYAMA ET AL.
Office Action Summary	Examiner	Art Unit	
	CRISTINA SHERR	3685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>7/17/'08</u>.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1,2 and 5-38</u> is/are pending in the application.
     4a) Of the above claim(s) <u>7,13-16,18-27,29-33,35 and 36</u> is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1,2, 5-6,8-12,17,28,34 and 36</u> is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
     a) ☐ All   b) ☐ Some * c) ☐ None of:
         1. ☐ Certified copies of the priority documents have been received.
         2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
     Paper No(s)/Mail Date <u>06/12/08</u>
4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____ .

DETAILED ACTION

1.   This Office Action is in response to Applicant's Amendment filed July 17, 2008.

Claims 1-2, 5-38 are currently pending in this case. Claims 3-4 have been previously

canceled. Claims 7, 13-16, 18-27, 29-33, and 37-38 are withdrawn. Claims 1, 2, 6, 17,

28, and 36 are currently amended. Claims 1, 2, 5-6, 8-12, 17, 28, 34 and 36 are

currently under examination.

Continued Examination Under 37 CFR 1.114

2.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 17,

2008 has been entered.

Information Disclosure Statement

3.   The information disclosure statement (IDS) submitted on June 4, 2008 is in

compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure

statement is being considered by the examiner.

Response to Arguments

4.   Applicant's arguments, filed July 17, 2008, with respect to the section 112

rejections of the claims have been fully considered and are persuasive. The section

112 rejection has been withdrawn.

5.   Applicant's arguments with respect to the section 103 rejections of the claims, as currently amended, have been considered but are moot in view of the new ground(s) of rejection.

Remarks

6.   While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function alone. MPEP 2114; *In re Swineheart*, 169 USPQ 226; *In re Schreiber*, 44 USPQ2d 1429 (Fed. Cir. 1997). a recitation with respect to the material intended to be worked upon by a claimed apparatus does not impose any structural limitations upon the claimed apparatus which differentiates it from a prior art apparatus satisfying the structural limitations of that claimed. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

7.   In this case, we find that a Central Processing Unit, or CPU, is hardware, and therefore an apparatus or device. We further find that a module license of a program is clearly software or data, and therefore not part of what the apparatus is, but rather what it does. The same is found with respect to buffers, keys, access conditions, etc. Therefore, thee features do not serve to further distinguish the claims from the prior art.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9.   Claims 1-2, 5-6, 8-12, 17, 28, 34 and 36 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Hashimoto et al (US 2001/0018736).

10.   Regarding claim 1 -

11.   Hashimoto discloses a central processing unit executing a program(e.g. abs, par

0004, 0078) comprising an encrypting unit encrypting a block (e.g. 0069, 0074) , and

decrypting an encrypted block (e.g. par 0079, fig.2), wherein: a first private key is

concealed in secrecy (e.g. par 0075); and said encrypting unit obtains from a first

license a code decryption key for decrypting an encrypted block which configures a first

program by decrypting with the first private key the first license of the first program (e.g.

par 0074), which is encrypted with a public key pairing with the first private key (e.g. par

0075);

the code decryption key is recorded to said tamper resistant buffer (par 0147),

the first license includes an access condition used when an execution process of the

first program accesses a memory region, and wherein said central processing unit

further includes:

           a Translation Lookaside Buffer (TLB) recording an address of the

memory region, at which the encrypted block which configures the first program is

recorded, and the access condition to the memory region (par 80),

           a memory-managing unit (par 0080),

           a cache (par 144), and.

           a processor core ((par 0144),

           wherein said TLB and said tamper resistant buffer are linked (par 144),

wherein said memory managing unit obtains the access condition to the memory region from said TLB based on an address or a memory region, at which an encrypted block is recorded, and further obtains the code decryption key corresponding to the memory region from said tamper resistant buffer (par 146),

wherein said processor core determines whether an access to the memory region is permitted to be made from the execution process based on the access condition obtained by process if said processor core determines that the access to the memory region is permitted to be made (par 247) and,

wherein said encrypting unit writes to said cache a code obtained by decrypting the encrypted block within the memory region with the code decryption key obtained by said memory managing unit. (par 146).

12.   Hashimoto does not use the same terminology, as the instant application, "secret key" rather than "private key", but such differences in terminology do not confer patentability. It would be obvious t o one of ordinary skill in the art to adapt terminology to suit the needs of the users.

13.   Regarding claim 2 –

14.   Hashimoto discloses the central processing unit wherein said encrypting unit decrypts the encrypted block in units of cache when the encrypted block which configures the first program is output from a memory region to said cache (fig.8 par 0172).

15.   Regarding claim 5 –

16.   Hashimoto discloses a central processing unit wherein the code decryption key

and the encryption key used to encrypt the encrypted block are a same key (e.g. par

0049).

17.   Regarding claim 6 –

18.   Hashimoto discloses a central processing unit wherein when a memory region

accessed from the execution process of the first program switches from a first memory

region to a second memory region, said memory managing unit further determines

whether or not a code decryption key corresponding to the first memory region, which is

obtained from said tamper resistant buffer, and a code decryption key corresponding to

the second memory region match, and an access is made to the second memory region

from the execution process if said memory managing unit determines that the code

decryption keys match, or the access to the second memory region is not made from

the execution process if said memory managing unit determines that the code

decryption keys mismatch. (e.g. 0094).

19.   Regarding claim 8 –

20.   Hashimoto discloses the central processing unit wherein: a different data

encryption key is recorded to said tamper resistant buffer for each code decryption key;

said encrypting unit records data within said cache to the memory region that is

corresponded to the data decryption key by said TLB after encrypting the data with the

data decryption key when recording the data to the memory region, and writes

encrypted data within the memory region to said cache after decrypting the read data

with the data encryption key when reading the encrypted data within the memory region
(e.g. par 0050).

21.   Regarding claim 9 –

22.   Hashimoto discloses a central processing unit wherein when data obtained by
executing a first code is used by a second code, said processor core sets said TLB so
as to provide the second code with an access right to a memory region to which the
data is recorded, and also sets said TLB and said tamper resistant buffer so that the
second code uses a data encryption key for encrypting the data when reading the data
from the memory region (e.g. par 0090).

23.   Regarding claim 10 –

24.   Hashimoto discloses a central processing unit further comprising: a register; and
a register access control table for performing access control for said register, wherein
said processor core controls sealing and release of said register with a sealing flag
within said register access control table (e.g. par 0145).

25.   Regarding claim 11 –

26.   Hashimoto discloses a central processing unit wherein when contents of said
TLB is recorded to a page table within an external storage device, said encrypting unit
affixes a signature to the contents to be recorded, and verifies whether or not the
signature is legal when contents of the page table is captured into said TLB. (e.g. par
0147).

27.   Regarding claim 12 –

28.   Hashimoto discloses a central processing unit wherein when contents of said

tamper resistant buffer is recorded to an encryption key table within an external storage

device, said encrypting unit encrypts the contents to be recorded. (e.g. par 0147).

29.   Regarding claim 17 –

30.   Hashimoto discloses a central processing unit wherein: said tamper resistant

buffer records unable-to-output information indicating whether or not to output

corresponding information within said tamper resistant buffer to an outside of said

tamper resistant buffer, and cache lock information indicating whether or not to output

corresponding information to an outside of said cache; and a move of the first license

between the first program and a different program is managed based on the unable-to-

output information and the cache lock information. (e.g. par 0180).

31.   Claims 28, 34, and 36 are rejected under the same criteria as above.

32.   Examiner's note: Examiner has cited particular columns and line numbers in

the references as applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings in the art and are

applied to the specific limitations within the individual claim, other passages and figures

may be applied as well. It is respectfully requested from the applicant, in preparing the

responses, to fully consider the references in entirety as potentially teaching all or part

of the claimed invention as well as the context of the passage as taught by the prior art

or disclosed by the examiner.

Conclusion

33.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to CRISTINA SHERR whose telephone number is (571)272-6711. The examiner can normally be reached on 8:30-5:00 Monday through Friday.

34.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Calvin L. Hewitt, II can be reached on (571)272-6709. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CRISTINA OWEN SHERR/   CRISTINA OWEN SHERR
Examiner, Art Unit 3685   Examiner
                                                                     Art Unit 3685